REMARKS

In the Office Action mailed June 7, 2007 the Examiner rejected all pending claims, namely, Claims 1-27. The Applicants request entry of the amendments listed above and consideration of the following remarks. The Applicants have amended Claims 8, 10, and 13-14. In addition, the Applicants request a one month extension of time. Each rejection is discussed below in relation to each independent claim. Reconsideration is respectfully requested.

Rejections

The Examiner rejected Claims 1-3, 5-8, 10, 12-14, 16-19, 21-22, 24-25 and 27 under 35 U.S.C. § 103(a) as being unpatentable over the Takenouchi reference (JP 06-338793) in view of the Yoshida reference (U.S. Publication No. 202/0039894). Each independent claim is discussed below.

Claim 1

The Examiner asserts that Claim 1 is obvious based on the Takenouchi reference in view of the Yoshida reference. In response, the Applicants request reconsideration in view of the following remarks. The Applicants submit that the Examiner is misinterpreting the Takenouchi reference by interpreting its teaching too broadly.

The Applicants disagree that the Takenouchi reference teaches the following claim elements from Claim 1.

> *processing the first signal to reduce harmonic cross-coupling thereby creating a processed first signal;*
>
> and
>
> *processing the second signal to reduce harmonic cross-coupling thereby creating a processed second signal;*

These elements require that processing occur on the signal output from the synthesizer, such as the PLL, to reduce harmonic cross-coupling. As a point of perspective, these claimed operation steps process the first signal and second signal, which are the signals output from the synthesizers. The signals created by the processing, i.e. the processed first signal and the processed second signal, are then provided to the switch, as is claimed.

When citing the Takenouchi reference, the Examiner cites drawing 1 and paragraph 8 of the Takenouchi reference. With regard to Drawing 1, it is at best confusing and the Applicants submit that it teaches very little. A portion of Drawing 1 is in Japanese and further, the switch 42 is only shown as receiving input form the PLL 33 and the CPU. As such, this drawing do not meet the claim limitations because the switch 42 only receives the signal from on PLL. In addition, the translated text barely qualifies as comprehensible. As such, the Applicants submit that it would be difficult if not impossible for one of ordinary skill in the art to be taught from this reference. The Applicants request that this be taken into consideration. The Applicants attorney has made a best attempt to to read and interpret this foreign reference.

In addition, in Figure 1 the only physical elements between the PLL 32 34, which is the synthesizer, and the switch are elements 34, 36, and 38 in the upper path and 35, 37, and 39 in the lower path. None of these elements however, perform processing to reduce harmonic cross-coupling. As such, Drawing 1 can not teach these claim elements. Each element is now discussed.

Elements 34, 35 and elements 36, 37 are low pass filters (paragraph 0017) which filter the PLL output, but these filters do not reduce harmonic cross-coupling nor does the Takenouchi reference provide such teaching. As set forth in the text of paragraph 0020, the low pass filters 34, 35, 36, 37 modify the error signal into an error voltage, which is provided to the VCO. This is part of the generation of the first signal and the second signal, which are provide to the switch because the filter output is simply the voltage creation circuit to drive the VCO.

Elements 38, 39 are voltage controlled oscillators (VCO) which is an element that generates the first signal and the second signal as claimed. It is well understood that the VCO does not reduce harmonic cross-coupling but actually is part of the synthesizer that generates the desired frequency. As a result, the apparatus taught by Drawing 1 does not each the operation steps set forth above.

With regard to paragraph 8 cited by the Examiner, it is re-typed for reference below.

> *[0008]*
> *[Problem(s) to be Solved by Invention] However, if it was in such a conventional PLL frequency synthesizer circuit formed into many circuits, by having formed many circuits, interference of the signal by the oscillator circuit of each PLL frequency circuit increased, and there was a trouble that spurious (interference noise) one will occur or the consumed electric current will increase. In order to prevent interference of a signal, a cure, such as shielding each oscillator-circuit section etc. or fully preparing spacing of each synthesizer, is needed. Moreover, although there are approaches, such as stopping the current supply to VCO, of those who are not using it to increase of the consumed electric current by having formed many circuits, when approaches, such as stopping the current supply to VCO, are taken, there is a fault of taking time amount until it takes the time amount to the oscillation at the time of a rebot or a frequency becomes stable.*

This paragraph, which is part of the background, discusses the problems solved by the Takenouchi reference but it in no way discloses the claim elements set forth above. A paragraph in a prior reference that discusses problems in the prior art does not provide teaching for each and every method for solving those problems. The fact of the matter is that the Takenouchi reference teaches a different way of solving the problem, namely, shielding each oscillator circuit, spacing to reduce coupling, and shutting down a VCO which is not in use. (paragraph 8 and 0013). Where in paragraph 0008 is it taught to process the output of the synthesizer to reduce cross-coupling before switching? Shielding and increased spacing do not meet the

limitation of processing the signal and shutting down a VCO is not processing, but indeed, just the opposite.

As a result, the Applicants submit that paragraph 8 does not teach these claim elements and that Claim 1, and the claims that depend there from are allowable.

Claim 8

The Applicants have amended Claim 8 to require limit processing of the first signal, second signal, or both. The prior art cited by the Examiner does not teach limit processing. The Examiner asserts that the PLL performs limit processing, but this is an unsupported assertion that is technically incorrect. A PLL is a phase lock loop configured to tracks a frequency. Limit processing is discussed at and supported by paragraphs 056, 057, 058, and 062 of the present application is different. The Applicants request that the Examiner review these specific paragraphs and reconsider the rejection of Claim 8 in view of this claim limitation. The Applicants request allowance of Claim 8 and the claims which depend from Claim 8.

Claim 14

The Examiner rejected Claim 14 based on the same teachings as discussed above for Claim 1 and 8. The Applicants have amended Claim 14 to require a multiplier or divider before the switch. Paragraph 042 provides support for this limitation and the technical basis that signals that are at frequencies which are at non-integer multiples induce less cross-coupling. The Takenouchi reference does not teach this element. The Yoshida reference, which is cited for teaching a divider, does not teach a divider before the switch and after the switch as is claimed in Claim 14.

In addition, the divider circuit of the Yoshida reference is within the frequency synthesizer 10A (paragraph 0064 defines element 10A as the synthesizer). Thus, the divider is part of the frequency synthesizer 10A i.e. signal generator, but Claim 14 as amended also requires a frequency modification device and a divider, which is not taught by the Yoshida

reference in combination with the Takenouchi reference. In particular, the Yoshida reference in combination with the Takenouchi reference does not teach a frequency modification device after the switch and dividers/multipliers before the switch. For these reasons, the Applicants request allowance of Claim 14 and the claims that depend from Claim 14.

Claim 22

Claim 22 is submitted as being allowable because neither the Takenouchi reference nor the Yoshida reference teach a frequency modification device configured to modify the frequency of a signal output from a switch. The Takenouchi reference does not teach a frequency modification device after the switch, i.e. to receive the switch output. The Yoshida reference does not teach a frequency modification device after the switch 18. In the Yoshida reference, the devices 6, of Figure 6 is a phase shift element which does not change the frequency. Since neither reference teaches a frequency modification device after the switch the Applicants submit that Claim 22 is allowable.

In addition, to the extent there is a divider in the system of the Yoshida reference, it is part of the synthesizer 10 and not a device in addition to a signal generator as is claimed. As set forth in paragraph 052 of the present application, the synthesizer (signal generator 504, 512) of the present application also includes a multiplier or divider. As such, that is simply inherently part of the synthesizer (signal generator) and not a separate element after the switch as claimed. For this additional reason, the Applicants request allowance of Claim 22 and the claims that depend from Claim 22.

SUMMARY

Applicant asserts that Claims 1-27 are in a condition for allowance and respectfully requests a notice as to the same. If any matters remain outstanding, the Examiner is invited to contact the undersigned by telephone.

Respectfully submitted,

Dated: 9/18/07 By: C. Miller

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